A NEW PILOT RESEARCH FACILITY FOR HJT AND SELECTIVE CONTACT SOLAR CELLS – PV-TEC SELECT

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ABSTRACT: After 10 years of operation of its Photovoltaic Technology Evaluation Centre PV-TEC Fraunhofer ISE recently significantly expanded its research capabilities with the opening of a new pilot research facility for selective contact solar cells – PV-TEC SELECT. PV-TEC SELECT aims to address major challenges on the way to industrialize high efficiency solar cell concepts like Heterojunction (HJT) or TOPCon technology. In this context, the paper introduces the new research facility with its unique equipment setup and process environment (Clean room class 1000 on more than 800 m²). The development of a robust base line process allows Fraunhofer ISE to expand its research offerings for PERC solar cells to next generation high efficiency cell concepts like HJT and TOPCon.

Keywords: Pilot production, Selective Contacts, Heterojunction, Throughput, Inline processing

1 INTRODUCTION

The race for higher efficient PV modules generates an increasing level of complexity in the processes involving the manufacturing of more sophisticated products and hence the increase in related investment & fabrication costs. Given that the market still requires a reduction of the technology cost, a difficult equation has to be solved: to produce high efficiency industrial devices with a low industrial processing costs. Among the existing solar cell technologies, selective contacts, especially the Heterojunction Technology (HJT), have demonstrated a large potential to address these challenges. Furthermore, the HJT solar module is specifically suited for a bi-facial architecture, further enhancing the electricity production capacity by 15-20%, and opening up many new market segments. The HJT technology will remain during the next decade one of the premium technologies with 1-2% higher efficiency than conventional technologies. In order to support the development of this technology and 10 years of successful operation of our existing Pilot Research platform PV-TEC (Photovoltaic Technology Evaluation Centre) [1], Fraunhofer ISE decided to expand its current technical infrastructure to set up a new pilot facility for solar cells based on selective contacts – PV-TEC-SELECT. The new centre was officially inaugurated in spring 2016 and has been step-wise expanded since then. It is expected to reach full operation at the end of Q1/2018. Within this new facility, companies along the entire production chain to produce highest efficient solar cells can find an optimum framework to test their latest process and equipment innovations on an industrial relevant scale.

The main goal of PV-TEC SELECT is to capitalize on previous lab-based developments on the hetero-junction and selective contact technology and bring the key selected technologies to industrial-scale production level leveraging the potential of a high level of automation to further reduce production costs. We present the design of the service centre that has the goals to offer service at high volume production rates, to be able to compare new and existing production technologies for selective contacts and that is able to be flexibly extended in the future and is able to evaluate upcoming new solar cell processing sequences for highest efficient solar cell structures on an industrial scale outside the industrial production facilities.

2 CHALLENGES IN MANUFACTURING AND AMBITION

PV-TEC SELECT addresses services and R&D topics on relevant existing bottlenecks for industrial scale production of HJT/selective contact solar cells:

- Quality assurance: Incoming inspection of source wafer material becomes mandatory in order to keep overall production performance distributions tight. Focussed parameters to be determined include base resistivity and minority carrier lifetime distributions.
- Defectivity and interface sensitivity: One of the major limitations and cost drivers in current high efficiency production of HJT cells are all necessary efforts to keep wafers clean in between the critical surface sensitive processing steps while keeping wafer throughputs high. R&D efforts concentrate on suitable automation solutions and process ambient specifications as well as alternative process sequences to reduce vacuum breakages and automation needs.
- Throughput: Optimizing productivity is essential to stay cost competitive. Increasing the throughput of the equipment in order to achieve maximum output is therefore a suitable way to reduce tool-related costs per cell. In order to optimize the throughput in a HJT cell production line, both, front-end (chemical and deposition processes) and back-end (metallization and classification) processes should have equal capacity. Current ITRPV expects wafer throughputs per tool of more than 5000 wafer/h from 2019 onwards [2]
- OPEX and CAPEX cost: Efforts to reduce cost sensitive materials like wet chemical solutions or silver pastes for front (and rear) metallisation by decreasing finger width, alternative and/or simplified process sequences showing similar or even superior performance need to be investigated.

For the formation of selective contacts, two basic approaches are followed and further developed at Fraunhofer ISE. They can be separated by the maximum temperature allowed during processing.

The low temperature approach (T_{max} < 250°C) represents the classical Heterojunction solar cell process comprising of the deposition of intrinsic amorphous silicon for surface passivation.
Within the high temperature approach (T_{max} > 250°C), Fraunhofer ISE further develops its proprietary and patented TOPCon technology. For TOPCon, surface passivation is achieved by tunneling oxide deposition followed by the formation of doped micro- or poly-crystalline silicon layers on both sides.
In both cases, metallization includes TCO deposition and screen-printed, PVD or plated front and rear metallization techniques, in the high temperature case much wider process windows offer advantages over the rather limited process conditions for classical HJT.

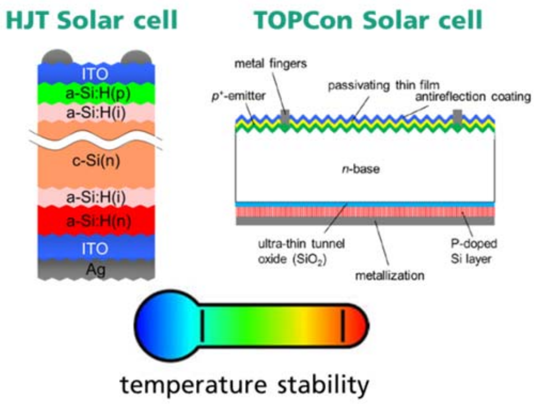

Figure 1: Main device structures for development within PV-TEC SELECT.

3 FACILITY LAYOUT AND SERVICE OFFERINGS

PV-TEC SELECT host the full front end processing chain for HJT and selective contact solar cell structure comprising of inline and batch wet chemistry tools, inline as well as cluster tool based PECVD deposition for intrinsic and doped amorphous and microcrystalline silicon layers as well as PVD deposition of TCO, metal as well as metal oxide layers (Figure 3). The corresponding processing equipment has been selected to be able to operate at higher throughputs (500-1000 Wafer/h) in order to allow design of experiments on statistically relevant data base.
The laboratory environment has been designed to fulfil Cleanroom Class 1000 conditions which allow us to easily switch process sequences without sacrificing the cleanliness of wafer surfaces in-between the different processing steps.
The front end processing within PV-TEC SELECT is well connected with the backend technologies in our already existing PV-TEC pilot line exhibiting different printing based metallisation techniques (screen print, dispensing, inkjet, flexographic print) [3-5] as well as plating technologies. Additionally, the activities are strongly linked to our Module Technology Centre, where cell connection and encapsulation of the new device structures and metallization approaches are tested and qualified. The design of the new evaluation centre is based on the assumption that a solid baseline process for Heterojunction solar cells is needed as reference process and technology set. To be able to further develop the solar cell processes and to implement future concepts like the TOPCon technology [6], the baseline equipment is supplemented with innovative components.

In PV-TEC SELECT the machines are organised as (mostly) automated islands. The major processing tools are:

- Batch wet etching tool for texturing and cleaning
- in-line wet etching tool for cleaning and conditioning
- Reference DC parallel plate PECVD system for intrinsic and doped amorphous silicon layer deposition
- Inductively coupled plasma (ICP)-PECVD system for intrinsic and doped amorphous silicon as well as PECVD based TCO layers
- Inline linear-rf based multi-chamber PECVD system for intrinsic and doped amorphous silicon layers
- Tube LPCVD system for the deposition of doped poly-Si layers
- Tube PECVD system for the deposition of doped poly-Si layers
- PVD cluster system for DC and rf biased sputtering of TCOs, metals and metal oxide layers
- Inline PVD systems comprising DC and rf biased sputtering of TCOs as well as metal oxide layers

The following main service areas are addressed and offered:

- Testing of new equipment in PV-TEC SELECT by bypassing the baseline.
- Solar cell producers should be able to bypass their line and execute interesting processes.
- Equipment suppliers that do not have a complete production line should be able to order partly processed wafers for testing their equipment which can remain at the supplier's site. Finalizing can be done at ISE.
- Qualifying materials e.g wafers, pastes, chemicals.
- Training of foreign staff

4 BASELINE PROCESS

Figure 2, Table 1 and 2 show recent achievements in back end processing to establish a baseline printing based process on well-known industrial-like equipment, enabling for short process times and a high-throughput production capability [3].

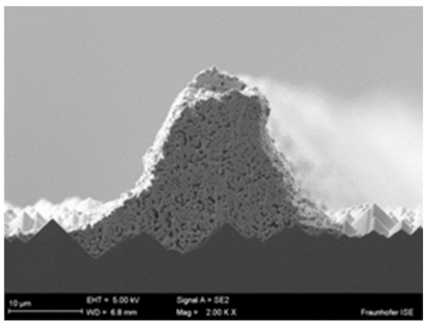

Figure 2: SEM images of contact lines screen-printed with a low-temperature silver paste: double printed line with $w_{f,\varnothing}$ = 34 µm and $h_{fmax,\varnothing}$ = 20 µm

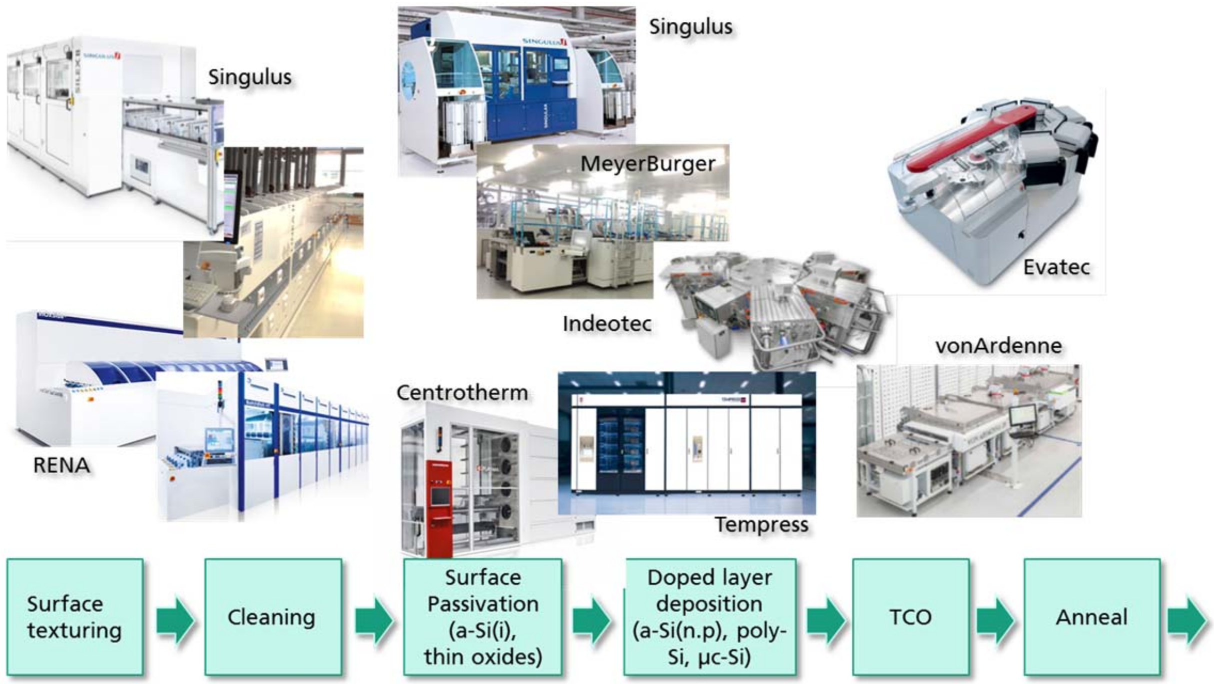

Figure 3: Equipment setup of new Pilot Research Facility PV-TEC SELECT

Screen printing as state-of-the-art metallization technique has shown its ability to produce fine contact fingers on SHJ solar cells. Dispensing is a promising alternative, as it also can be used for the conventional module integration based on busbars, but offers higher aspect ratios even within a single printing step (Table 1). Heterojunction solar cells with a conversion efficiency of up to 21.9 % and FF > 80 % were produced by single screen printing on bothcell sides. Although, highest Fill Factor values of 80.9 % were reached with the dispensing method, increased shading caused by higher printed line width as well as a different busbar geometry led to decreased values of J_{sc}, still enabling an efficiency of 21.6% (Table 2). The high level of V_{oc} proves that the passivation quality is not significantly affected by both metallization techniques.

Table I: Comparison of achieved printed line geometry for all investigated printing methods

	$w_{f,\varnothing}$ (µm)	$h_{fmax,\varnothing}$ (µm)	*AR* (u.a.)
Screen-printing (single print, 50 µm)	56	13	0.23
Screen-printing (double print, 30 µm)	34	20	0.59
Dispensing	68	30	0.44

Table II: I-V-data of the best screen-printed compared to the best dispensed solar cell. Decreased J_{sc} of the dispensed solar cell is partly due to a different busbar geometry causing a loss of ~0.5 mA/cm²

	V_{oc} (mV)	J_{sc} (mA/cm^2)	*FF* (%)	η (%)
Screen-printing (single print)	727	37.6	80.1	21.9
Dispensing	726	36.9	80.9	21.6

4 SELECTED RESEARCH RESULTS

4.1 Quality assurance throughout the process chain

Important quality requirement for wafers is needed to assure solar cell conversion efficiency improvements and process robustness for the pilot line activities, therefore incoming inspection of source wafer material becomes mandatory in order to keep overall production performance distributions tight. Within PV-TEC SELECT, wafer fine inspection of large area n-type silicon source wafers can be performed within a fully automated inline inspection tool determining all basic geometrical, electronic as well as optical parameters of each individual wafer.

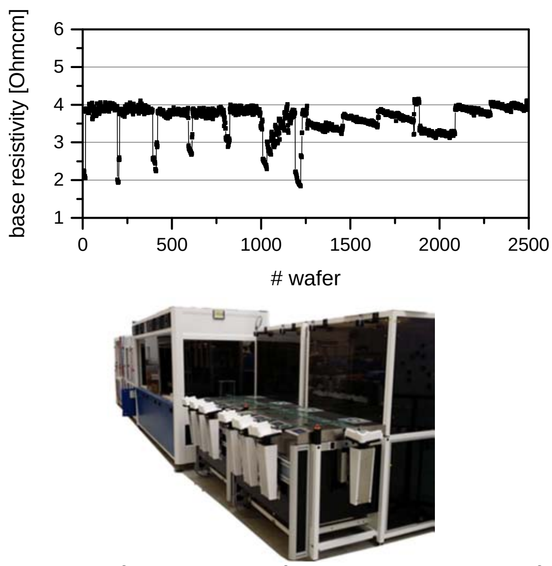

Figure 4: Lifetime example for incoming inspection of large batch of n-type silicon source wafers measured by fully automated inline inspection system: distribution of base resistivity

4.2 Wafer handling of highly sensitive wafer surfaces

One of the major challenges for the industrialization of high efficiency solar cell manufacturing processes represents the automation and handling of the wafers with their highly sensitive surfaces. As typical wafer throughputs of industrial process tools surpass 3600 wafers/h, wafer handling cycles (loading/unloading from cassettes or carriers) need to be performed typically in the range of only a few seconds. Common gripper solutions like Bernoulli, suction or area grippers all show an impact on the resulting electrical properties at critical process interfaces e.g. for wafer handling in between the final surface clean from a batch wet bench and the intrinsic amorphous silicon deposition within a typical PECVD furnace. Earlier studies showed an impact of up to 10 % lifetime reduction in the related areas due to the handling step [7], which in case of HJT solar cells could result in significant losses in the open circuit voltage. In case of Bernoulli grippers, mainly the deposition of particles is responsible.

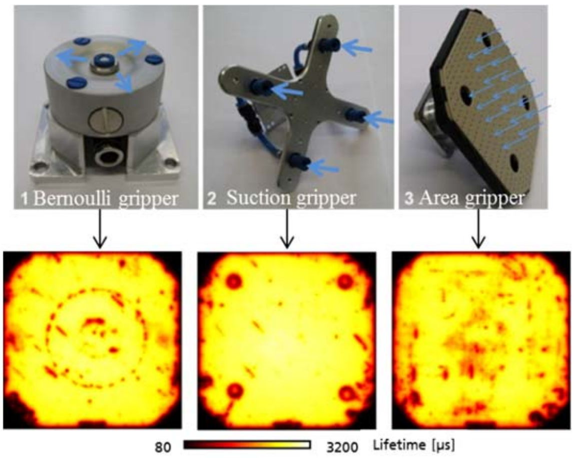

Figure 5: Investigations on the impact of wafer grippers on electrical properties of alkaline textured and a-Si passivated surfaces [7]

The "fingerprint" reflects the distribution of the Bernoulli stream nozzles that blows the air from the inside to the outside to create a lower pressure of the Bernoulli Effect [8]. Future investigations will further concentrate on optimization of Bernoulli based wafer gripping as well as investigations on other touchless wafer transport and handling methods like ultrasonic end-effectors.

4.3 Technologies with high throughput potential

Aiming to address the higher throughput demand of future processing lines (and to reduce the cost of ownership (COO)) processes for the deposition of hydrogenated amorphous silicon (a-Si:H) which is used as passivation and selective layer for silicon heterojunction (SHJ) solar cells are developed on a state-of-the-art inline PECVD deposition system MAiA..The developed processes have to fulfill two important basic requirements:

- excellent passivation of the c-Si absorber
- high selectivity with respect to the charge carriers to obtain the best possible electrical contact.

The a-Si:H(i) process supplies excellent stability concerning passivation even after chamber cleaning by an etching process and although to the fact that other processes carried out within the same deposition chamber. In Figure 6 the minority carrier lifetime τ_{eff} is shown over a larger period of tool operation. One can see a fluctuation of the τ_{eff}, but an overall level of above 3 ms (corresponding to an iV_{OC} >730 mV)..

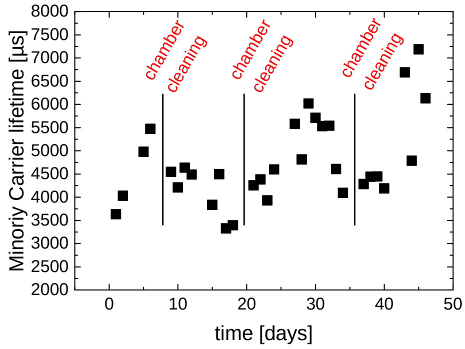

Figure 6: Minority carrier lifetime as a function of the time to proove the reproducibility/stability of the a-Si:H(i) process; red lines show chamber cleaning cycles by an etching process [9].

Fig. 7 depicts the result for the iV_{OC} as a function of the wafer position on the deposition tray. It can be seen that with an optimized process iV_{OC} values over 730 mV were obtained for all positions whereby a slight degradation in transport direction (from top to bottom) can be observed.

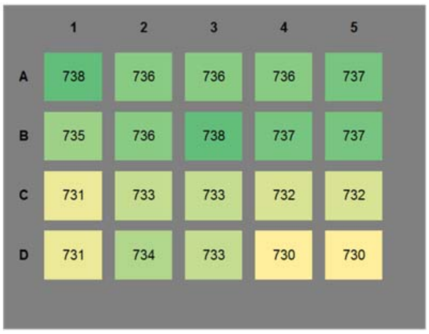

Figure 7: Scheme of the inline deposition tray (5 columns, 4 rows) with iV_{OC} values in mV measured by QSSPC as a function of the tray position [9].

Further results also for n- and p-doped amorphous silicon layers by inline PECVD deposition are presented elsewhere [9]

4.4 New process technologies for cost reduction

In Figure 8, results of a new, simple, cost effective and production-feasible ozone-based surface conditioning process for the controlled rounding and smoothing of textured surfaces is presented [10]. For the rounding of the textured surface a diluted solution consisting of HF and HCl in ozonized DI-H_2O was utilized which additionally offers an improved cleaning performance. The process was carried out in an industrial batch tool. The ozone concentration is kept constant during the process by continuous recirculation through an ozone generator which is coupled with the process bath. Within this experiment the degree of rounding was adjusted by varying the exposure time (2, 4 and 8 min). Considering the impact of the rounding reaction on the size of the pyramids, n-type Cz samples with small size (1-3 µm) and medium size pyramids (4-6 µm) were prepared in potassium hydroxide (KOH) solution in addition with a commercial available organic two component additive. For all c-Si surfaces already the 2 min O_3 treatment resulted in significantly higher efficiencies compared to the standard SC1/SC2 clean.

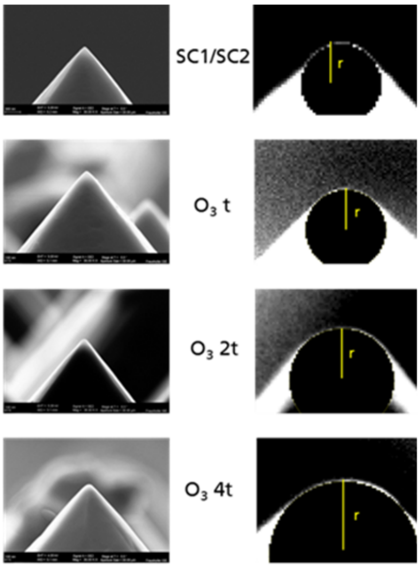

Figure 8: Ozone based surface treatments after texturing (two different pyramid sizes) in comparison to a standard SC1/SC2 clean. The resulting rounding of the pyramid tips was analyzed by high resolution SEM (35 K optical zoom) with manual fitting of a circle in the rounded structure of the pyramid tip in order to estimate the „Rounding radius“.

The O_3-based conditioning leads to a cell efficiency improvement of up to 0.4% absolute for the group with small size pyramids and up to 0.8% to maximum values of 22.7% for the medium size pyramids. The results demonstrate the importance of an adequate c-Si surface treatment, which can be obtained with industrially feasible approaches. The results are an important step towards lowering the cost of advanced cell concepts while at the same time increasing the cell efficiency.

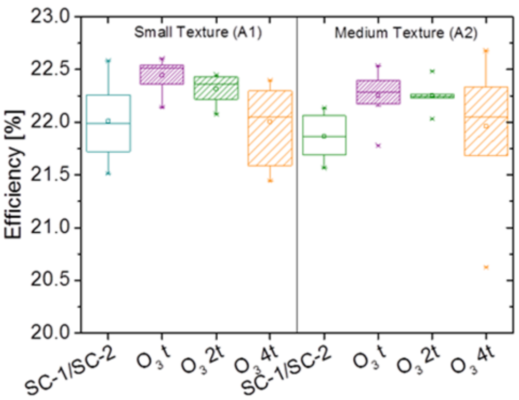

Figure 9: Solar cell efficiency comparison of large area HJT cells with different Ozone based surface treatments after texturing.

One major drawback of state-of-the-art screen printed based metallization approaches for HJT solar cells represents the low temperature anneal requirement which typically leads to rather poor line conductivities of the fine front metallization grid resulting in higher series resistance losses. At Fraunhofer ISE, a new metallization has been developed based on Laser induced forward transfer (LIFT) of metals to form a fine line seed layer for subsequent selective copper and silver plating to form the contact [11]. An additional thin insulating layer needs to be deposited on top of the TCO in order to protect the TCO during plating. Excellent finger geometries and electrical properties have been achieved using this metallization approach (Figure 10). First application of the process sequence for large area (156 x 156 mm²) HJT solar cells revealed an absolute increase in efficiency of 0.4 %mainly due to an improvement in fill-factor as well as J_{sc}.

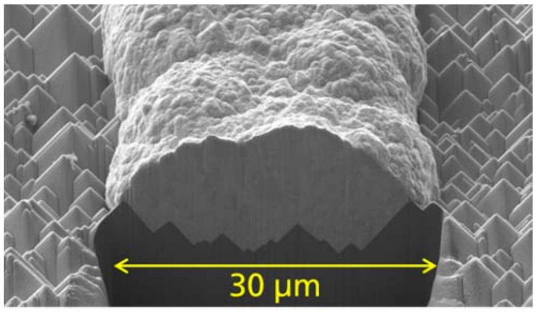

Figure 10: SEM image of cross section of Laser transferred seed-layer and Cu-plated contact finger.

Table III: I-V-data of the best screen-printed compared to the best LIFT process

Metallization	Area [cm²]	V_{oc} [mV]	J_{sc} [mA/cm²]	FF [%]	η [%]
Screen printing	239,0	726	37,7	79,0	21,6
Screen printing	239,0	727	37,8	79,1	21,7
LIFT + Cu-plating	239,0	727	38,2	79,7	22,1
LIFT + Cu-plating	239,0	728	38,0	80,1	22,2

5 CONCLUSION

We have set up a complete pilot line for the front end of solar cells with selective contacts. On an area of more than 900 m² we reach a clean-room quality of 1000, this unique set-up enables to us to perform high efficiency solar cell processing with very high standards for surface cleanliness while still applying individual industrial type systems for the deposition of highly passivating layers. The individual tool set up allows performing research for different potential device structures like HJT or TOPCon in order to find optimum industrial applicable process sequences.

The main systems include: inline and wet etching tools for texturing and cleaning, an ICP PECVD as well as a inline linear rf PECVD tool for intrinsic and doped amorphous silicon layers as well as a PVD tool for DC and rf biased deposition of TCOs.

In the different relevant research areas (wet chemistry for surface texture and cleaning, deposition of amorphous silicon, TCO layers) we have achieved excellent resulzs enabling cell efficiencies for HJT well above 22 %.

We combine "this" with the state-of-the-art back-end processing in our main PV-TEC facility which has approved to process heterojunction solar cells at an efficiency exceeding 22% on high-throughput equipment in a rather pilot lab ambient

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